

10/08/11

ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

U.S. **UTILITY** Patent Application

<p>O.I.P.E.</p> <p>SCANNED <u>Am</u> Q.A. <u>Am</u></p>	<p>PATENT DATE</p>
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APPLICATION NO. 09/989667	CONT/PRIOR	CLASS 710	SUBCLASS 305	ART UNIT 2181	EXAMINER Aure
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APPLICANTS

Francis Joseph

TITLE

System-On-Chip architecture that utilizes FeRAM and re-configurable hardware

PTO-204
12/99

ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____	_____ (Assistant Examiner)		NOTICE OF ALLOWANCE MAILED	
	_____ (Date)			
	_____ (Primary Examiner)		ISSUE FEE	
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<input type="checkbox"/> The terminal ____months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		ISSUE BATCH NUMBER	
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